

CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of reading data from a memory array comprising:

transferring data from a memory module onto an input/output signal line; and

sensing the data based on a capacitance of said input/output signal line.
2. The method of claim 1 further comprising delaying the sensing of the data based on the capacitance of said input/output signal line.
3. The method of claim 2, wherein a delay for an input/output signal line with a capacitance greater than a threshold is greater than a delay for an input/output signal line with a capacitance less than the threshold.
4. The method of claim 3, wherein multiple sensing of said less capacitive input/output signal lines is increased.
5. The method of claim 1 further comprising the act of shutting off a control signal controlling a sense amplifier that receives a signal from a low capacitance input/output signal line in a time less than a time for shutting off a high capacitance input/output signal line.
6. A column output delay circuit for a memory device comprising:

a first delay device, said first delay device delaying a column enable signal for a first period of time; and

a second delay device, said second delay device delaying a column enable signal for a second period of time.

7. The circuit of claim 6, wherein said first delay device delays a sensing operation on an input/output signal line having less capacitance, and an accumulation of said first and second delay device delays a sensing operation on an input/output signal line having greater capacitance.

8. The circuit of claim 6 further comprising a first column enable signal produced by said first delay device, and a second column enable signal produced by a combination of said first and second delay device.

9. A memory device comprising:

a memory array;

a datapath coupled to said memory array by input/output signal lines;
and

a column output delay circuit, said circuit coupled to sense amplifiers in said datapath for controlling, based on a capacitance of a particular input/output signal line, when the particular input/output signal line is sensed by said sense amplifiers.

10. The device of claim 9 further comprising:

output data pads for transmitting data from said memory array; and

combinatorial logic for determining which sense amplifier sends data to said output pads.

11. The device of claim 9, wherein said column output delay circuit comprises a first delay device that delays a sensing operation on an input/output signal line of a first capacitance, and a second delay device wherein an accumulation of said first and second delay device delays a sensing operation on an input/output signal line having a second capacitance greater than said first capacitance.

12. The device of claim 11, wherein said column output delay circuit further comprises a first column enable signal produced by said first delay device, and a second column enable signal produced by a combination of said first and second delay device.

13. The device of claim 12, wherein said first and second column enable signals control said sense amplifiers.

14. A processor system comprising:

a processor; and

a memory device, said memory device comprising:

a memory array,

a datapath coupled to said memory array by input/output signal lines, and

a column output delay circuit, said circuit coupled to sense amplifiers in said datapath for controlling, based on a capacitance of a particular input/output signal line, when the particular input/output signal line is sensed by said sense amplifiers.

15. The system of claim 14, wherein said column output delay circuit comprises a first delay device that delays a sensing operation on an input/output signal line having a first capacitance, and a second delay device wherein an accumulation of said first and second delay device delays a sensing operation on an input/output signal line having second capacitance which is greater than said first capacitance.

16. The system of claim 15, wherein said column output delay circuit further comprises a first column enable signal produced by said first delay device, and a second column enable signal produced by a combination of said first and second delay device.

17. The system of claim 16, wherein said first and second column enable signals control said sense amplifiers.